Abstract of the Disclosure

A method and apparatus for pausing execution of instructions from a thread is described. In one embodiment, a pause instruction is implemented as two instructions or microinstructions: a SET instruction and a READ instruction. When a SET flag is retrieved for a given thread, the SET instruction sets a Bit flag in memory indicating that execution for the thread has been paused. The SET instruction is placed in the pipeline for execution. The following READ instruction for that thread, however, is prevented from entering the pipeline until, the SET instruction is executed and retired (resulting in a clearing of the Bit flag). Once the Bit flag has been cleared, the READ instruction is placed in the pipeline for execution. During the time that processing of one thread is paused, the execution of other threads may continue.

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